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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
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ART UNIT	**PAPER NUMBER**
2822	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/678,609	HONDA, HIROKAZU	
	Examiner	Art Unit	
	David E. Graybill	2822	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 February 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *18-21,27-43,45-54 and 86-89* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *18-21,27-43,45-54 and 86-89* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *3 pages*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Claims 86-89 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. The undescribed subject matter is the limitation, "a metallic frame formed in said side of said first surface."

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 18-21 and 27-42 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

In claims 18, 27, 29, 32, 36 and 37 the word "means" is preceded by the words "buffer layer" in an attempt to use a means clause to recite a claim element as a means for performing a specified function. However, since no function is specified by the words preceding "means," it is impossible to determine the equivalents of the element, as required by 35 U.S.C. 112, sixth paragraph. See *Ex parte Klumb*, 159 USPQ 694 (Bd. App. 1967). To further clarify, if "buffer layer means" is restated as "means for

buffer layering," the phrase makes no sense because the term "buffer layering" has no functional connotation, and the phrase is indefinite.

In the rejections infra, generally, reference labels are recited only for the first recitation of identical claim elements.

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 18-20 and 27-37 are rejected under 35 U.S.C. 103(a) as being unpatentable over the combination of Allen (4705205) and Hayashi (JP11238972).

At column 1, line 10 to column 2, line 20; column 2, lines 46-68; column 3, lines 42-49; column 4, lines 1-21; column 7, lines 9-25; column 8, line 32 to column 9, line 16; column 12, line 22 to column 13, line 46; column 13, line 66 to column 14, line 38; column 15, lines 8-45; column 16, lines 27-39; column 16, line 52 to column 17, line 18; column 18, lines 15-20; column 18, line 66 to column 19, line 16; column 20, lines 37-58; and column 21, lines 12-28, Allen discloses a semiconductor device comprising: an interconnection board 32 having first and second surfaces; at least one external electrode pad 10 in said interconnection board, said at least one

external electrode pad having an exposed surface; at least a semiconductor chip mounted on said interconnection board; and buffer layer means 20 having a first surface in contact with said second surface of said interconnection board and a second surface on which at least one external electrode 28 is provided, said buffer layer means for providing at least one electrical contact between said one external electrode pad and said at least one external electrode and for absorbing and/or relaxing a stress applied to said at least external electrode to make said interconnection board free from application of said stress; wherein said at least external electrode comprises plural external electrodes; wherein said buffer layer means comprises plural generally column shaped electrically conductive layers, each of which has a first end fixed to an external electrode pad 10 of said interconnection board and a second end directly fixed said external electrode; wherein said plural generally column shaped electrically conductive layers are made of a metal; wherein said buffer layer means comprises plural generally column shaped electrically conductive layers, each of which has a first end fixed to an external electrode pad of said interconnection board and a second end directly fixed said external electrode; and a stress absorption layer 22 filling gaps between said plural generally column shaped electrically conductive layers, and said stress absorption layer surrounding said plural generally

column shaped electrically conductive layers so that said stress absorption layer is in tightly contact with said plural generally column shaped electrically conductive layers; wherein said plural generally column shaped electrically conductive layers are made of a metal; wherein said stress absorption layer is made of an organic insulative material; wherein said buffer layer means comprises plural generally column shaped electrically conductive layers, each of which has a first end fixed to an external electrode pad of said interconnection board and a second end directly fixed said external electrode; a supporting plate 22 having plural holes, into which said plural generally column shaped electrically conductive layers with said external electrodes are inserted, and said supporting plate extending in parallel to said second surface of said interconnection board to form an inter-space between said supporting plate and said second surface of said interconnection board; and a supporting sealing resin material 22 filling said inter-space and surrounding both said plural generally column shaped electrically conductive layers and parts of said external electrodes so that said supporting sealing resin material is in tight contact with said plural generally column shaped electrically conductive layers and said parts of said external electrodes for supporting said external electrodes; wherein said

supporting sealing resin material is capable of absorbing and/or relaxing a stress applied to said external electrodes; wherein said plural generally column shaped electrically conductive layers are made of a metal; wherein said supporting sealing resin material is made of an organic insulative material; a supporting layer 34 on said second surface of said buffer layer means for supporting said external electrode; wherein said supporting layer further comprises: a supporting plate 22 having plural holes into which holes said external electrodes are inserted, and said supporting plate extending in parallel to said second surface of said buffer layer means to form an inter-space between said supporting plate and said second surface of said buffer layer means; and a supporting sealing resin material 22 filling said inter-space and surrounding parts of said external electrodes so that said supporting sealing resin material is in tight contact with said parts of said external electrodes for supporting said external electrodes.

However, Allen does not appear to explicitly disclose the external electrode pad buried in the interconnection board, and having the exposed surface level with the second surface so that the second surface and the exposed surface form a single flat plane, or wherein said interconnection board comprises a multilayer interconnection board having a multilevel interconnection structure.

Nonetheless, in the English abstracts and figures, Hayashi discloses an external electrode pad 2 buried in an interconnection board 1, and having the exposed surface level with a second surface so that the second surface and the exposed surface form a single flat plane, wherein the interconnection board comprises a multilayer interconnection board having a multilevel interconnection structure. Furthermore, it would have been obvious to combine the product of Hayashi with the product of Allen because it would provide the interconnection board of Allen as a multilayer interconnection board having long-term stability and superior moistureproofness.

Claims 21 and 38-42 are rejected under 35 U.S.C. 103(a) as being unpatentable over the combination of Allen and Hayashi as applied to claims 18-20 and 27-37, and further in combination with Tsukamoto (5841194).

The combination of Allen and Hayashi does not appear to explicitly disclose; wherein said external electrode comprises a solder ball; wherein said at least semiconductor chip is bonded via bumps to said first surface of said interconnection board; a sealing resin material provided on said first surface of said interconnection board for sealing said at least semiconductor chip and said bumps; at least a heat spreader provided on said at least semiconductor chip; an under-fill resin material provided on said first surface

of said interconnection board for sealing said at least semiconductor chip and said bumps; a stiffener spaced from at least one peripheral edge of said semiconductor chip; and a heat spreader contacting said semiconductor chip and said stiffener.

Nonetheless, at column 4, line 59 to column 8, line 61, Tsukamoto discloses a semiconductor device wherein an external electrode comprises a solder ball "solder balls"; a semiconductor chip 201 is bonded via bumps 204 to a first surface of an interconnection board 101; a sealing resin 205 material provided on the first surface of the interconnection board for sealing the semiconductor chip and the bumps; at least a heat spreader 701 provided on said at least semiconductor chip; an under-fill resin material 205 provided on the first surface of the interconnection board for sealing the at least semiconductor chip and the bumps; a stiffener 106 spaced from at least one peripheral edge of said semiconductor chip; and a heat spreader contacting said semiconductor chip and said stiffener. Moreover, it would have been obvious to combine the product of Tsukamoto with the product of the applied prior art because it would provide a chip carrier having improved manufacturing yield.

Claims 43, 45 and 50-54 are rejected under 35 U.S.C. 103(a) as being unpatentable over the combination of Nakamura (6372547) and Hsuan (6252300).

At column 5, line 55 to column 8, line 9; and column 10, line 49 to column 12, line 35, Nakamura discloses a semiconductor device comprising: an interconnection board 3 having first and second surfaces; at least one external electrode pad 11 buried in said interconnection board, said at least one external electrode pad having an exposed surface level with said second surface so that said second surface and said exposed surface form a single flat plane; a buffer layer 20, 24 having a first surface contacting said second surface of said interconnection board; a supporting plate 55 spaced from a second surface of said buffer layer and defining a gap between said second surface of said buffer layer and said supporting plate, said supporting plate having plural holes therein "hole portions"; at least one external electrode 54 in one of said holes in said supporting plate and connected to said at least one external electrode pad through said buffer layer; and a sealing resin 50 in said gap and surrounding and supporting said at least one external electrode; wherein said external electrode comprises a solder ball.

To further clarify the disclosure of a buffer layer 20, 24 and a supporting plate 55, the terms "buffer" and "supporting" are statements of

intended use of the layer and plate, respectively, that do not appear to result in a structural difference between the claimed layer and plate and the layer and plate of Nakamura. Further, because the layer and plate of Nakamura appear to have the same structure as the claimed layer and plate, they appear to be inherently capable of being used for the intended uses – specifically, for buffering and supporting, respectively, and the statements of intended use do not patentably distinguish the claimed layer and plate from the layer and plate of Nakamura. The manner in which a product operates is not germane to the issue of patentability of the product; Ex parte Wikdahl 10 USPQ 2d 1546, 1548 (BPAI 1989); Ex parte McCullough 7 USPQ 2d 1889, 1891 (BPAI 1988); In re Finsterwalder 168 USPQ 530 (CCPA 1971); In re Casey 152 USPQ 235, 238 (CCPA 1967). And, claims directed to product must be distinguished from the prior art in terms of structure rather than function. In re Danley, 120 USPQ 528, 531 (CCPA 1959). "Apparatus claims cover what a device is, not what a device does [or is intended to do]." Hewlett-Packard Co. v. Bausch & Lomb Inc., 15 USPQ2d 1525, 1528 (Fed. Cir. 1990).

Also, Nakamura discloses that the external electrode 54 comprises a solder ball because Nakamura discloses, at least in the cited Figures 6B, 6C,

6D and 7, that the external electrode comprises a round or roundish, cylindrical solder body.

However, Nakamura does not appear to explicitly disclose at least a semiconductor chip mounted on said first surface of said interconnection board; wherein said at least semiconductor chip is bonded via bumps to said first surface of said interconnection board.

Notwithstanding, at column 4, lines 37-53, Hsuan discloses at least a semiconductor chip 74 mounted on said first surface of said interconnection board 74; wherein said at least semiconductor chip is bonded via bumps 60 to said first surface of said interconnection board. Moreover, it would have been obvious to combine these disclosures of Hsuan and Nakamura because it would provide a stacked chip package having reduced size and increased reliability.

Claims 46-49 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nakamura and Hsuan as applied to claim 43, and further in combination with Nakatani (6038133).

As cited, Nakamura and Hsuan disclose a sealing material "underfill" provided on said first surface of said interconnection board for sealing said at least semiconductor chip and said bumps; at least a heat spreader 60 provided on said at least semiconductor chip; an under-fill "underfill"

material provided on said first surface of said interconnection board for sealing said at least semiconductor chip and said bumps; an inherent stiffener 20 spaced from at least one peripheral edge of said semiconductor chip; and a heat spreader contacting said semiconductor chip and said stiffener.

To further clarify, the term "heat spreader" is a statement of intended use of the product that does not appear to result in a structural difference between the claimed product and the product of the applied prior art. Further, because the product of the applied prior art appears to have the same structure as the claimed product, it appears to be inherently capable of being used for the intended use - specifically, for spreading heat - and the statement of intended use does not patentably distinguish the claimed product from the product of the applied prior art. The manner in which a product operates is not germane to the issue of patentability of the product; Ex parte Wikdahl 10 USPQ 2d 1546, 1548 (BPAI 1989); Ex parte McCullough 7 USPQ 2d 1889, 1891 (BPAI 1988); In re Finsterwalder 168 USPQ 530 (CCPA 1971); In re Casey 152 USPQ 235, 238 (CCPA 1967). Also, "Expressions relating the apparatus to contents thereof [in the instant case - heat] during an intended operation are of no significance in determining patentability of the apparatus claim."; Ex parte Thibault, 164 USPQ 666, 667

(Bd. App. 1969). And, claims directed to product must be distinguished from the prior art in terms of structure rather than function. In re Danley, 120 USPQ 528, 531 (CCPA 1959). "Apparatus claims cover what a device is, not what a device does [or is intended to do]." Hewlett-Packard Co. v. Bausch & Lomb Inc., 15 USPQ2d 1525, 1528 (Fed. Cir. 1990).

However, Nakamura and Hsuan do not appear to explicitly disclose a sealing resin material and an under-fill resin material.

Notwithstanding, at column 9, lines 22-31, Nakatani discloses an underfill sealing resin material. Furthermore, it would have been obvious to combine this disclosure of Nakatani with the disclosure of Nakamura and Hsuan because it would facilitate provision of the under-fill of Nakamura and Hsuan and prevent the formation of gaps.

Claims 50-51 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nakamura and Hsuan as applied to claim 43, and further in combination with Kitazawa (6057600).

As cited supra, Nakamura and Hsuan disclose wherein said buffer layer comprises plural generally column shaped electrically conductive layers 24 that connect said at least one external electrode to said at least one external electrode pad; and an inherently supporting sealing material 20 surrounding said plural generally column shaped electrically conductive layers so that

said supporting sealing material is in tight contact with said plural generally column shaped electrically conductive layers; wherein said supporting sealing material is inherently capable of absorbing and/or relaxing a stress applied to said at least one external electrode; wherein said plural generally column shaped electrically conductive layers are made of a metal "Cu"; wherein said supporting sealing resin material is made of an insulative material.

However, Nakamura and Hsuan does not appear to explicitly disclose a supporting sealing resin material made of an organic insulative material.

Still, as cited supra, Nakamura and Hsuan disclose a glass-ceramic supporting sealing material wiring board 20. In addition, at column 11, lines 3-9, Kitazawa discloses that a glass-ceramic wiring board 23 and an organic insulative resin wiring board 23 are alternatives and equivalents; therefore, it would have been obvious to substitute or combine the board of Kitazawa for or with the board of Nakamura and Hsuan. See In re May (CCPA) 136 USPQ 208 (It is our opinion that the substitution of Wille's type seal for the cement of Hallauer in Figure 1 would be obvious to persons of ordinary skill in the art from the disclosures of these references, merely involving an obvious selection between known alternatives in the art and the application of routine technical skills.); In re Cornish (CCPA) 125 USPQ 413; In re Soucy

(CCPA) 153 USPQ 816; Sabel et al. v. The Wickes Corporation et al. (DC SC) 175 USPQ 3; Ex parte Seiko Koko Kabushiki Kaisha Co. (BdPatApp&Int) 225 USPQ 1260; and Ex parte Rachlin (BdPatApp&Int) 151 USPQ 56. See also Smith v. Hayashi, 209 USPQ 754 (Bd. of Pat. Inter. 1980) (However, there was evidence that both phthalocyanine and selenium were known photoconductors in the art of electrophotography. "This, in our view, presents strong evidence of obviousness in substituting one for the other in an electrophotographic environment as a photoconductor." 209 USPQ at 759.). An express suggestion to substitute one equivalent component or process for another is not necessary to render such substitution obvious. In re Fout, 675 F.2d 297, 213 USPQ 532 (CCPA 1982). "It is prima facie obvious to combine two compositions each of which is taught by the prior art to be useful for the same purpose, in order to form a third composition to be used for the very same purpose.... [T]he idea of combining them flows logically from their having been individually taught in the prior art." In re Kerkhoven, 626 F.2d 846, 850, 205 USPQ 1069, 1072 (CCPA 1980) (citations omitted). See also In re Crockett, 279 F.2d 274, 126 USPQ 186 (CCPA 1960); Ex parte Quadranti, 25 USPQ2d 1071 (Bd. Pat. App. & Inter. 1992).

Claims 86-88 are rejected under 35 U.S.C. 103(a) as being unpatentable over the combination of Tsukamoto (5841194), Maeno (6222738) and Hayashi (JP11238972).

As cited supra, Tsukamoto discloses a semiconductor device comprising: a multilayer interconnection board 108 having first and second surfaces being the same surface; an external electrode pad 102 formed in a side of said second surface; a semiconductor chip 201 mounted in a side of said first surface; a metallic post 204 protruding from said external electrode pad; a metallic frame 106 formed in said side of said first surface to surround said metallic post, a gap being thereby formed between said metallic post and said metallic frame; and a layer 205 filling said gap; wherein said external electrode pad has an exposed surface forming a substantially flat plane; wherein a height of said metallic post from said second surface is substantially equal to a height less than the total height of said metallic frame from said second surface.

However, Tsukamoto does not appear to explicitly disclose a resin layer.

Still, at column 6, lines 45-51, Maeno discloses a resin layer 11. In addition, it would have been obvious to combine these disclosures of Maeno

and Tsukamoto because it would facilitate provision of the layer 205 of Tsukamoto.

Also, Tsukamoto does not appear to explicitly disclose that the electrode pad has an exposed surface forming a substantially flat plane with the second surface.

Notwithstanding, as cited supra, Hayashi discloses this limitation. Furthermore, it would have been obvious to combine these disclosures of Tsukamoto and Hayashi because it would provide the interconnection board 108 of Tsukamoto as a multilayer interconnection board having long-term stability and superior moistureproofness.

Applicant's amendments and remarks filed 2-17-5; 8-3-4 and 5-11-4 have been fully considered, are addressed by the rejections supra, and are further addressed infra.

Applicant traverses the 35 U.S.C. 112, second paragraph rejection of claims 18-21 and 27-42 because, "The "for" is not at the beginning of the element definition, there is no requirement for such grammatical construction."

This traversal is respectfully deemed unpersuasive because the claims are not rejected because there is a requirement that the "for" be at the beginning of the element definition. Also, the function specified by the

words following the word "means" does not correct the lack of functional connotation of the phrase "buffer layer means." In order to continue to afford applicant the benefit of compact prosecution, it is suggested that changing the phrase "buffer layer means" to "buffer means" would overcome this rejection.

Also, applicant contends that, in claim 18, the phrase "means for" is not modified by sufficient structure, material or acts for achieving the specified function; therefore, the USPTO should apply 35 U.S.C. 112, sixth paragraph.

This contention is respectfully deemed moot in light of the 35 U.S.C. 112, second paragraph rejection of claim 18 for the phrase "buffer layer means," because the function is not clearly specified and is indeterminable.

Applicant also argues that, "The solder performs 28 . . . column structure is not the same or equivalent to the layer structure of the present invention. The columns are tall and thin."

This argument is respectfully deemed unpersuasive because it is unsupported by evidence. Also, the argument is respectfully traversed because, as elucidated in the rejections, any differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious. To this end, the USPTO will not

apply 35 U.S.C. 112, sixth paragraph until the 35 U.S.C. 112, second paragraph rejection of claims 18, 27, 29, 32, 36 and 37 for the phrase "buffer layer means" is overcome. Therefore, the claims are not limited to structure not recited in the claims, e.g. columns that are not tall and thin. In any case, as disclosed at column 7, lines 9-25, Allen discloses columns that are not tall and thin.

The art made of record and not applied to the rejection is considered pertinent to applicant's disclosure. It is cited primarily to show inventions similar to the instant invention.

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

For information on the status of this application applicant should check PAIR:
Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Alternatively, applicant may contact the File Information Unit at (703) 308-2733. Telephone status inquiries should not be directed to the examiner. See MPEP 1730VIC, MPEP 203.08 and MPEP 102.

Any other telephone inquiry concerning this communication or earlier communications from the examiner should be directed to David E. Graybill at (571) 272-1930. Regular office hours: Monday through Friday, 8:30 a.m. to 6:00 p.m.
The fax phone number for group 2800 is (703) 872-9306.

David E. Graybill
Primary Examiner
Art Unit 2827

D.G.
9-May-05